REMARKS

Claims 11-18 are pending in the present application. Claims 11-13, 15, 16 and 18 have been amended.

Claim Rejections-35 U.S.C. 102

Claims 11 and 15-17 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Bechade et al. reference (U.S. Patent No. 5,430,387). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The output buffer circuit of claim 11 includes in combination a pull up control circuit "connected to the input terminal, the pull up control circuit including a delay circuit that is connected to the input terminal and that has third inverters connected in series that provide a delayed input signal, the pull up control circuit pulling up a voltage of the first signal under control of the delayed input signal during a predetermined time from a time when the input signal is changed from "L" level to "H" level...". Applicant respectfully submits that the Bechade et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has interpreted circuit elements 140, 146 and 158 in Fig. 2 of the Bechade et al. reference collectively as the pull up control circuit of claim 11, transistors 110 and 106 as the first inverter of claim 11, and transistor 102 as the first output transistor of claim 11. With respect to claim 15, the Examiner has interpreted P/FET

transistor 140 in Fig. 2 of the Bechade et al. reference as a pull up transistor.

However, as featured in claim 11, the pull up control circuit includes a delay circuit that is connected to the input terminal of the circuit, whereby the delay circuit includes third inverters connected in series that provide a delayed input signal. Applicant respectfully submits that Fig. 2 of the Bechade et al. reference does not include third inverters connected in series that provide a delayed input signal that controls pulling up of a voltage of a first signal, **in addition to** transistors 110 and 106 which have been interpreted by the Examiner as the first inverter of claim 11.

Moreover, as described beginning in column 4, line 17 of the Bechade et al. reference, voltage for turn-on is supplied to transistor 102 (interpreted by the Examiner as the first output transistor of claim 11), by a pull-up predrive circuit 138 consisting of N/FET transistor 106 and P/FET transistor 140. Transistors 106 and 140 act in opposition to control the turn-on of transistor 102 by controlling the voltage supplied to transistor 102 at gate 108. A reference voltage at node 142 is supplied to transistor 140 at gate 144 by an AC voltage reference circuit 146 that includes voltage divider network 148. As further described in column 5, lines 13-15 of the Bechade et al. reference, voltage divider 148 supplies a reference voltage at node 142 which turns on transistor 140, to control the turn-on of transistor 102.

As noted above, the Examiner has interpreted P/FET transistor 140 as a pull up transistor. However, as emphasized in the above noted portions of the Bechade et al. reference, transistor 140 in Fig. 2 of the Bechade et al. reference is controlled to pull up

transistor 102 responsive to a reference voltage provided by voltage divider 148 at node 142. Transistor 140 in Fig. 2 of the Bechade et al. reference is not controlled by a delayed input signal provided by a delay circuit having third inverters connected in series. Accordingly, Applicant respectfully submits that the output buffer circuit of claim 11 distinguishes over the Bechade et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 11 and 15-17, is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claim 18 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Bechade et al. reference in view of the Popat et al. reference (U.S. Patent No. 5,804,990). Applicant respectfully submits that the Popat et al. reference as secondarily relied upon does not overcome the above noted deficiencies of the Bechade et al. reference. Applicant therefore respectfully submits that claim 18 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, for at least these reasons.

Allowable Subject Matter

Applicant notes the Examiner's acknowledgment that claims 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Responsive to the acknowledgment of allowable subject matter, claims 12 and 13 have been respectively amended to be in independent form as including the features of base claim 11, merely to advance prosecution of this application. Accordingly, the Examiner is respectfully requested to acknowledge that claims 12-14 are allowed.

Conclusion

Since claims 12 and 13 have been amended merely to be in independent form and thus respectively have the same scope as previously pending claims 12 and 13, the amendments to claims 12 and 13 should not be construed as narrowing scope within the meaning of *Festo*.

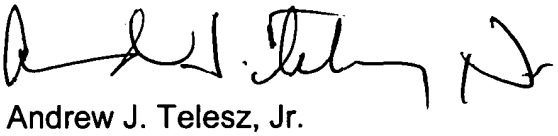
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740